AMENDMENTS TO THE SPECIFICATION

Please replace the present title with the following amended title:

SEMICONDUCTOR MEMORY DEVICE PROVIDED WITH ERROR CORRECTING CODE CIRCUITRY

Please replace the paragraph on page 12 bridging to page 13 of the specification, beginning with "Next, configurations of ..." with the following amended paragraph:

Next, configurations of the encoding circuits 11 in the ECC circuit 9 corresponding to the Hamming Code (12, 8) SEC that the semiconductor memory device has are described by referring to Fig. 2. Each of the encoding circuits 11 (here, two pieces of the encoding circuits 11) is so constructed as to have a syndrome tree 20 configuration in which 8 bits of information bits D0 to D7 are input from each of the input bus lines 6A and 6B ~~and, when the test signal TB1 is fed to four pieces of AND circuits 21A to 21D and ten pieces of exclusive OR circuits (EOR) 22A to 22J~~, four pieces of AND circuits 21A to 21D and ten pieces of exclusive OR circuits (EOR) 22A to 22J are connected so as to produce such a 5 relationship as shown in Fig. 2, the test signal TB1 is fed to four pieces of AND circuits 21A to 21D. Moreover, each of the encoding circuits 11 is so configured that it produces, by arithmetic operations, 4 bits of parity bits PO to P3 and outputs them which allow the ECC circuit 9 to make a specified error correction according to contents of the input 8 bits of the information bits D0 to D7. The 8 bits (4 bits x 2) of the parity bits output from two pieces of the encoding circuits 11 are written in the parity bit area 3 in the memory array 1 through a write buffer (WB) 10A and the input/output

gates 16. In Fig. 2, a generator matrix "G" shown in its upper part is produced by arithmetic operations so that it becomes the generator matrix "G" shown just below in its lower part when a test signal TBl = L (low) level.

Please replace the paragraph on page 17 bridging to page 18 of the specification, beginning with "(2) Then, the function ..." with the following amended paragraph:

(2) Then, the function test is carried out on the parity bit area 3 with the test signals TB1, ~~TB2~~ and TB3 as shown in Fig. 2 to Fig. 4 being set at the ~~H~~ L (~~high~~low) level and the test signal TB2 being set at the H (high) level to obtain the FMB. Thus, information is obtained about a state of distributions of fail bits of not only information bits but also parity bits. At this time, ~~three~~ four bits of information bits D0 to D3 are written into or read from the parity bit area 3 as ~~it~~ they are, however, all of the remaining information bits D4 to D7 are set at a L (low) level. Moreover, whenever necessary, the write buffers 10A and 10B or main amplifiers 19A and 19B are deactivated and a function test for a desired data pattern is performed on all bits.

Please replace the paragraph on page 18 of the specification, beginning with "(2) In a state in which ..." with the following amended paragraph:

(2) In a state in which the test signal TB2 in the decoding circuit 12 shown in Fig. 3 is set at the ~~L~~ H (~~low~~high) level, whereas the test signals TB1 and TB3 are set to the L (low) level, the long Pause Refresh test is carried out on the parity bit area 3 to obtain the FBM.